IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1-12 were cancelled in a previous response.

Claims 1-12 (cancelled)

13. (previously presented) A memory controller, comprising:

a) a host side region having a memory access request input and a memory command packet chunk output, a memory command packet chunk being a portion of a memory command packet, said host side region to be clocked by a first clock; and

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b) a memory side region having a memory command packet chunk input coupled to said memory command packet chunk output, said memory side region to be clocked by a second clock, said second clock different than said first clock.

14. (previously presented) The memory controller of claim 13 wherein said memory command packet chunk output further comprises a row output and a column output.

15. (previously presented) The memory controller of claim 13 wherein said host side region further comprises a scheduler coupled to said memory access request input, said scheduler configured to generate said memory command packet.

16. (previously presented) The memory controller of claim 15 wherein said scheduler is coupled to a queue.

17. (previously presented) The memory controller of claim 15 wherein said memory command packet can be a row command.

18. (previously presented) The memory controller of claim 15 wherein said memory command packet can be a column command.

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19. (previously presented) The memory controller of claim 15 wherein said scheduler further comprises logic to determine when resource conflicts may arise.

20. (previously presented) The memory controller of claim 13 wherein said host side memory controller region further comprises a second memory command packet chunk output.

21. (previously presented) The memory controller of claim 20 wherein said second clock is faster than said first clock.

22. (previously presented) The memory controller of claim 20 wherein said host side memory controller region is configured to present a second memory command packet chunk upon said second memory command packet chunk output,

said second memory command packet chunk a portion of a second memory command packet.

23. (previously presented) An apparatus, comprising:

a) a memory controller comprising a host side region and a memory side region, said host region having a memory access request input and a memory command packet chunk output, a memory command packet chunk being a portion of a memory command packet, said host side region to be clocked by a first clock, said memory side region having a memory command packet chunk input coupled to said memory command packet chunk output, said memory side region to be clocked by a second clock, said second clock different than said first clock; and

b) a DRAM memory coupled to said memory side region.

24. (previously presented) The apparatus of claim 23 further comprising an external agent configured to read and write to said DRAM memory via said memory controller.

25. (previously presented) The apparatus of claim 24 wherein said external agent further comprises a processor.

26. (previously presented) The apparatus of claim 24 wherein said external agent further comprises a graphics subsystem.

27. (previously presented) The apparatus of claim 24 wherein said external agent further comprises an expansion bus master.

28. (previously presented) The apparatus of claim 23 wherein said memory command packet chunk output further comprises a row output and a column output.

29. (previously presented) The apparatus of claim 23 wherein said host side memory controller region further comprises a scheduler coupled to said memory access request input, said scheduler configured to generate said memory command packet.

30. (previously presented) The apparatus of claim 29 wherein said scheduler is coupled to a queue.

31. (previously presented) The apparatus of claim 29 wherein said memory command packet can be a row command.

32. (previously presented) The apparatus of claim 29 wherein said memory command packet can be a column command.

33. (previously presented) The apparatus of claim 29 wherein said scheduler further comprises logic to determine when resource conflicts may arise.

34. (previously presented) The apparatus of claim 23 wherein said host side memory controller region further comprises a second memory command packet chunk output.

35. (previously presented) The apparatus of claim 34 wherein said second clock is faster than said first clock.

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36. (previously presented) The apparatus of claim 34 wherein said host side memory controller region is configured to present a second memory command packet chunk upon said second memory command packet chunk output, said second memory command packet chunk a portion of a second memory command packet.

37. (currently amended) A method, comprising:

a) ~~generated~~ generating a memory command packet from a memory request while clocked by a first clock; and

b) sending a memory command packet chunk to a memory controller region clocked by a second clock, a memory command packet chunk being a portion of said memory command packet, said second clock different than said first clock.

38. (previously presented) The method of claim 37 further comprising sending a second memory command packet chunk along with said memory command packet chunk, said second memory command packet chunk associated with a subsequent memory command packet.

39. (previously presented) The apparatus of claim 37 wherein said memory command packet further comprises a row command.

40. (previously presented) The apparatus of claim 39 wherein said row command activates a memory row.

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41. (previously presented) The apparatus of claim 39 wherein said row command precharges a memory row.

42. (Previously presented) The apparatus of claim 39 wherein said memory command packet further comprises a column command.

43. (previously presented) The apparatus of claim 39 wherein said column command is use to read from a DRAM memory device.

44. (previously presented) The apparatus of claim 39 wherein said column command is used to write to a DRAM memory device.

45. (previously presented) A memory controller, comprising:

a) a host side region to be clocked by a first clock, said host side region comprising:

(i) a queue to queue command packet chunks;

(ii) a plurality of memory command packet chunk output lanes stemming from steering circuitry, said steering circuitry to guide specific command packet chunks received from said queue to specific command packet chunk output lanes, said queue having an output for each output lane, said steering circuitry further comprising:

a) a first multiplexer having a first input to receive a first packet chunk from a queue output, said first multiplexer having a second input coupled to a latch circuitry output, said latch circuitry downstream from said queue output to hold a second packet chunk from said queue output;

b) a second multiplexer having a plurality of inputs, one of said inputs coupled to said first multiplexer's output, other inputs of said second multiplexer downstream from outputs of said queue other than said queue output; and,

b) a memory side region to be clocked by a second clock, said memory side region comprising:

inputs coupled to said memory command packet chunk output lanes.

46. (previously presented) The memory controller of claim 45 further comprising shift logic on said memory side region to receive memory command packet chunks from said memory side region inputs.

47. (previously presented) The memory controller of claim 45 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

48. (previously presented) The memory controller of claim 45 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

49. (previously presented) The memory controller of claim 45 further comprising a third multiplexer having a first input coupled to said queue output and a second input coupled to a path that propagates command packets chunks that do not enter said queue, said latch circuitry coupled to said third multiplexer's output to receive command packet chunks from said third multiplexer's output.

50. (previously presented) The memory controller of claim 49 wherein said third multiplexer further comprises a third input coupled to an output of said latch circuitry.

51. (previously presented) The memory controller of claim 45 wherein said steering circuitry further comprises a third multiplexer having a first input coupled an output of said second multiplexer, said third multiplexer having a second input coupled to a path that propagates command packets chunks that do not enter said queue.

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52. (previously presented) The memory controller of claim 51 further comprising logic circuitry between said third multiplexer and an output lane to insert a null packet chunk onto said output lane.

53. (previously presented) An apparatus, comprising:

a memory controller, comprising:

a) a host side region to be clocked by a first clock, said host side region comprising:

(i) a queue to queue command packet chunks;

(ii) a plurality of memory command packet chunk output lanes stemming from steering circuitry, said steering circuitry to guide specific command packet chunks received from said queue to specific command packet

chunk output lanes, said queue having an output for each output lane, said steering circutry further comprising:

a) a first multiplexer having a first input to receive a first packet chunk from a queue output, said first multiplexer having a second input coupled to a latch circuitry output, said latch circuitry downstream from said queue output to hold a second packet chunk from said queue output;

b) a second multiplexer having a plurality of inputs, one of said inputs coupled to said first multiplexer's output, other inputs of said second multiplexer downstream from outputs of said queue other than said queue output;

b) a memory side region to be clocked by a second clock, said memory side region comprising:

inputs coupled to said memory command packet chunk output lanes; and,

DRAM memory coupled to said memory side region of said memory controller.

54. (previously presented) The apparatus of claim 53 further comprising shift logic on said memory side region to receive memory command packet chunks from said memory side region inputs.

55. (previously presented) The apparatus of claim 53 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

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56. (previously presented) The apparatus of claim 53 wherein said steering circutry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

57. (previously presented) The apparatus of claim 53 further comprising a third multiplexer having a first input coupled to said queue output and a second input coupled to a path that propagates command packets chunks that do not enter said queue, said latch circuitry coupled to said third multiplexer's output to receive command packet chunks from said third multiplexer's output.

58. (previously presented) The apparatus of claim 57 wherein said third multiplexer further comprises a third input coupled to an output of said latch circuitry.

59. (previously presented) The apparatus of claim 53 wherein said steering circuitry further comprises a third multiplexer having a first input coupled an output of said second multiplexer, said third multiplexer having a second input coupled to a path that propagates command packets chunks that do not enter said queue.

60. (previously presented) The apparatus of claim 59 further comprising logic circuitry between said third multiplexer and an output lane to insert a null packet chunk onto said output lane.